

IN THE CLAIMS

What is claimed is:

- 5 1. A method for making a semiconductor device comprising:
 - forming on a substrate a dielectric layer that has a dielectric constant that is greater than the dielectric constant of silicon dioxide;
 - modifying the dielectric layer so that it will be compatible with a gate electrode to be formed on the dielectric layer; and then
- 10 forming a gate electrode on the dielectric layer.
2. The method of claim 1 wherein the dielectric layer is modified by:
 - forming a sacrificial layer on the dielectric layer;
 - transporting impurities from the dielectric layer to the sacrificial layer; then
- 15 removing the sacrificial layer.
3. The method of claim 2 wherein the dielectric layer is a high-k gate dielectric layer that has a dielectric constant that is greater than about 8.
4. The method of claim 3 wherein the high-k gate dielectric layer is formed by atomic layer chemical vapor deposition, and wherein the high-k gate dielectric layer comprises a material selected from the group consisting of hafnium oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, titanium oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

5. The method of claim 4 wherein the sacrificial layer comprises a titanium nitride layer.
6. The method of claim 5 wherein the titanium nitride layer is annealed to cause the impurities to be transported from the dielectric layer to the titanium nitride layer.
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7. The method of claim 6 wherein the gate electrode comprises polysilicon.
8. A method for making a semiconductor device comprising:
 - forming a high-k gate dielectric layer on a substrate, the high-k gate dielectric layer including impurities;
 - 10 forming a sacrificial layer on the high-k gate dielectric layer;
 - transporting the impurities from the high-k gate dielectric layer to the sacrificial layer; then
 - removing the sacrificial layer; and
 - 15 forming a layer that comprises polysilicon on the high-k gate dielectric layer.
9. The method of claim 8 wherein the sacrificial layer comprises a titanium nitride layer, and wherein the impurities are transported from the high-k gate dielectric layer to the titanium nitride layer by annealing the titanium nitride layer to getter the impurities from the high-k gate dielectric layer.
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10. The method of claim 9 wherein the substrate comprises silicon.

11. The method of claim 10 wherein the high-k gate dielectric layer is formed by atomic layer chemical vapor deposition, and is between about 20 angstroms and about 60 angstroms thick.

12. The method of claim 11 wherein the high-k gate dielectric layer 5 comprises a material selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide.

13. The method of claim 12 wherein the titanium nitride layer is between about 10 angstroms and about 50 angstroms thick.

14. The method of claim 13 wherein the titanium nitride layer is annealed by heating that layer at between about 500°C and about 10 1,000°C for between about 5 minutes and about 20 minutes.

15. The method of claim 14 wherein the titanium nitride layer is removed using a wet etch process that is selective for titanium nitride over the material used to make the high-k dielectric layer.

16. The method of claim 15 wherein the layer that comprises 15 polysilicon is between about 2,000 angstroms and about 4,000 angstroms thick.

17. A method for making a semiconductor device comprising:
forming a high-k gate dielectric layer on a substrate, the high-k gate dielectric layer being less than about 100 angstroms thick and comprising
20 a material selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide;

forming a titanium nitride layer that is between about 10 angstroms
and about 50 angstroms thick on the high-k gate dielectric layer;
annealing the titanium nitride layer at a temperature of between
about 500°C and about 1,000°C for between about 5 minutes and about
5 20 minutes; then
removing the titanium nitride layer;
forming a layer that comprises polysilicon on the high-k gate
dielectric layer; and
etching the polysilicon containing layer and the high-k gate
10 dielectric layer.

18. The method of claim 17 wherein the high-k gate dielectric layer is formed by atomic layer chemical vapor deposition and is between about 20 angstroms and about 60 angstroms thick.

19. The method of claim 18 wherein the titanium nitride layer is removed using a wet etch process that is selective for titanium nitride over the material used to make the high-k dielectric layer.

20. The method of claim 19 wherein the layer that comprises polysilicon is between about 2,000 angstroms and about 4,000 angstroms thick.

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